

17333

13141

3 Hours / 100 Marks

Seat No.

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- Instructions* –
- (1) All Questions are *Compulsory*.
 - (2) Answer each next main Question on a new page.
 - (3) Illustrate your answers with neat sketches wherever necessary.
 - (4) Figures to the right indicate full marks.
 - (5) Assume suitable data, if necessary.
 - (6) Use of Non-programmable Electronic Pocket Calculator is permissible.
 - (7) Mobile Phone, Pager and any other Electronic Communication devices are not permissible in Examination Hall.

Marks

1. a) Attempt any **SIX** of the following: **12**
- i) Define with respect to digital ICS.
 - 1) Propagation delay time
 - 2) Fan - Out
 - ii) State two advantages and disadvantages of digital system.
 - iii) State any four Boolean laws.
 - iv) State De-Morgan's first and second theorem.

P.T.O.

- v) Convert the following:
- 1) $(786)_{10} = (?)_2$
 - 2) $(624)_8 = (?)_2$
- vi) Draw logical symbol, truth table and logical expression of EX-OR gate.
- vii) Define priority encoders and name the following ICS.
- 1) IC 74147
 - 2) IC 74148
- viii) Define following with respect to DAC.
- 1) Resolution
 - 2) Settling time

b) **Attempt any TWO of the following:**

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- i) Convert the following:
- 1) $(AD5)_H = (?)_{10}$
 - 2) $(10110)_2 = (?)_{10}$
 - 3) $(625)_{10} = (?)_2$
 - 4) $(174)_{10} = (?)_{BCD}$
- ii) Implement OR and AND gates by using NAND gates only.
- iii) Perform following operation by using 2's complement method.
- 1) $(83)_{10} - (67)_{10}$
 - 2) $(53)_{10} - (97)_{10}$

2. Attempt any FOUR of the following: 16

- a) Draw logical symbol, truth table and logical expression for NAND and NOR gate.
- b) Simplify the following Boolean expressions using Boolean laws.
- i) $Y = A (\bar{A} + C) (\bar{A} B + \bar{C})$
- ii) $Y = B\bar{C}\bar{D} + \bar{A}BD + ABD + BC\bar{D} + \bar{B}CD + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}D$
- c) Differentiate between TTL, CMOS and ECL logic family w.r.t.
- i) Propagation delay
- ii) Noise margin
- iii) Fan out
- iv) Figure of merit.
- d) Minimize the following Boolean expression using K-map.
 $Y = \sum m (0, 1, 3, 4, 5, 6, 7, 13, 15)$
 Draw the logical ckt diagram of minimized expression using basic gates.
- e) Design full-adder using K-map, universal gates.
- f) Draw the block diagram of BCD to 7 - segment decoder / driver and draw its truth table.

3. Attempt any FOUR of the following: 16

- a) Reduce the following expression and implement it using logic gates.
 $Y = (\overline{AB} + \overline{A+B}) A \cdot \bar{B}$
- b) Draw the logical diagram of 1 : 4 demultiplexer and describe its working. Write the expression for the output and draw the circuit diagram using logic gates.
- c) Convert the expression $Y = AB + A\bar{C} + BC$ into the standard SOP form.

- d) For the given equation $F = BC + \bar{A} \bar{B} \bar{C} + AB \bar{C}$
- i) Simplify using K-map.
 - ii) Construct the simplified expression by using NAND gates only.
- e) Draw a schematic diagram of MS-JK flip flop. Explain its working with a truth table.
- f) Draw the logical circuit diagram of 3-bit synchronous counter. Describe its working with timing diagram.

4. Attempt any FOUR of the following: 16

- a) Draw the logical circuit of 4-bit serial - in serial - out shift register. Explain with truth table.
- b) Differentiate between combinational and sequential circuit (any four points).
- c) State the advantages and disadvantages successive approximation ADC.
- d) Draw a clock signal and explain positive edge triggering and negative edge triggering.
- e) Classify the memories and explain ROM.
- f) Draw the block diagram of dual slope A-D converters and describes its working.

5. Attempt any FOUR of the following: 16

- a) Perform the following BCD arithmetic operation:
 - i) $(637)_{10} + (463)_{10}$
 - ii) $(63)_{10} + (19)_{10}$
- b) Describe the significance of preset and clear terminals in J-K flip-flop.
- c) Reduce the following expression and implement logic gates.

$$Y = AB + ABC + AB(E + F)$$

- d) Draw circuit diagram of 4-bit asynchronous counter and describe with timing diagram.
- e) Draw the block diagram of comparator IC 7485 and write the truth table.
- f) Draw mod-11 asynchronous counter using T - flip-flop.

6. Attempt any TWO of the following: 16

- a) i) State the application of multiplexes. 2
 - ii) Design 1 : 16 DMUX using 1 : 4 DMUX 6
 - b) i) Convert S-R FF into D-FF and explain. 2
 - ii) Draw pin diagram of universal shift register IC 7495 and label it. 2
 - iii) State the applications of shift register. 4
 - c) i) Draw circuit diagram of weighted register method of D-A converter and explain in brief. 4
 - ii) Define the following specifications of A-D converter: 4
 - 1) Conversion time
 - 2) Resolution.
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