21415

17333

3 Hours/100 Marks

Seat No. | | | | | | | | |

Instructions : *(1)* ***All*** *questions are* ***compulsory.***
(2) Figures to the ***right*** *indicate* ***full*** *marks.*
(3) Mobile Phone, Pager and any other Electronic Communication devices are ***not permissible*** *in Examination Hall.*

MARKS

1. a) Attempt **any six** : **12**

   i) What is positive logic and negative logic in digital system ?

   ii) Define fan in and noise margin.

   iii) Draw symbol and truth table of 3 i/p OR gate.

   iv) State DeMorgan's theorem.

   v) Convert the following :

      a) $(156)_{10} \rightarrow (?)_{BCD}$ and $(?)_2$

   vi) List any four Boolean laws.

   vii) Define encoder. Write the number of IC used as decimal to BCD encoder.

   viii) Define any two specifications of ADC.

   b) Attempt **any two** : **8**

   i) Compare TTL and CMOS logic family on the basis of propagation delay, power dissipation, fan out and components used.

   ii) Design OR and AND gate using NOR gate only.

   iii) Perform the following binary subtraction using 2's complement :

      1) $(54)_{10} - (33)_{10} = ?$

      2) $(48)_{10} - (68)_{10} = ?$

P.T.O.

MARKS

2. Attempt **any 4** : **16**

a) Draw X-OR gate using NAND gate only. Also write O/P of each gate.

b) Simplify the following equation using boolean laws and realize it using basic gates only. $Y = ABC + A\overline{B}C + \overline{A}BC + \overline{A}\,\overline{B}C$.

c) Perform the following BCD arithmetic :

1) $(630)_{10} + (468)_{10}$

2) $(245)_{10} + (186)_{10}$.

d) Simplify the following equation using k-map and realize it using logic gates.
$Y = \Sigma m(0, 1, 2, 3, 8, 10) + \Sigma d(5, 7)$.

e) Design Half adder using k-map and basic gates.

f) Draw block diagram of decimal to BCD encoder and write its truth table.

3. Attempt **any four** : **16**

a) Simplify using DeMorgans theorem and realize it using basic gates.
$Y = \overline{(A\overline{B} + \overline{A}\overline{B})(AB + \overline{A}B)}$.

b) Design 8 : 1, MUX using 2 : 1 MUX and 4 : 1 MUX.

c) Minimize the following equation using k-map.

1) $Y = \Sigma m(0, 1, 2, 4, 5, 6)$

2) $Y = \Pi m(0, 2, 4, 5)$.

d) Design 1 : 8 demux using basic gates.

e) Explain different triggering methods used in f.f.

f) Explain working of PIPO with neat logic diagram and timing diagram.

MARKS

4. Attempt **any four** : **16**

   a) Explain working of 2 bit asynchronous counter with the help of neat diagram, truth table and timing diagram.

   b) Explain successive approximation type ADC with neat diagram.

   c) Describe working of RS ff using NANP gates only.

   d) What is race around condition ? How to eliminate it ?

   e) Define memory. Give classification of memory. Compare PROM and EPROM (any 2 pts.).

   f) What is the need of data converters ? List specifications of DAC.

5. Attempt **any four** : **16**

   a) Convert the following :

      1) $(366.54)_8 \rightarrow (?)_{10}$ and

      2) $(2015.32)_{10} \rightarrow (?)_{16}$.

   b) Compare combinational logic circuit and sequential logic circuit (any 4 pts.)

   c) Simplify the following and realize it.
   $Y = A + \overline{A}\,\overline{B}\,C + \overline{A}\,\overline{B}\,\overline{C} + ABC + \overline{A}\,\overline{B}$.

   d) Explain working of 3 bit synchronous counter with the help of neat logic diagram, timing diagram and truth table.

   e) Describe block diagram of digital comparator and write truth table of 2 bit comparator.

   f) Compare synchronous and asynchronous counter. (any 4 pts.)

6. Attempt **any two** : **16**

   a) i) Convert the following SOP equation into standard SOP equation. **2**
   $Y = AB + \overline{A}B + A\overline{B}\,\overline{C}$.

   ii) List any four applications of multiplexer and implement the following logic expression using 16:1 MUX. **6**
   $Y = \Sigma m(0, 3, 5, 6, 7, 10, 13)$.

MARKS

b) i) Draw symbol and truth table of negative edge triggered D.FF and positive edge triggered JK FF. **2**

ii) What is modulus of counter ? Show the method to determine the no. of flip flops for a mod-52 counter. **4**

iii) Draw only logic diagram of SIPO. **2**

c) i) A DAC has a full scale analog O/P of 10V and accepts 4 binary bits as i/ps. Find the voltage corresponding to each analog step. **4**

ii) Describe working of R-2R Ladder type DAC. **4**
