**MAHARASHTRA STATE BOARD OF TECHNICAL EDUCATION**
**(Autonomous)**
**(ISO/IEC - 27001 - 2005 Certified)**

**SUMMER-16 EXAMINATION**
**Model Answer**

**Subject Code: 17428** **Subject Name: Computer Hardware and Maintenance**

**Important Instructions to examiners:**

1) The answers should be examined by key words and not as word-to-word as given in the model answer scheme.
2) The model answer and the answer written by candidate may vary but the examiner may try to assess the understanding level of the candidate.
3) The language errors such as grammatical, spelling errors should not be given more Importance (Not applicable for subject English and Communication Skills).
4) While assessing figures, examiner may give credit for principal components indicated in the Figure. The figures drawn by candidate and model answer may vary. The examiner may give Credit for any equivalent figure drawn.
5) Credits may be given step wise for numerical problems. In some cases, the assumed Constant values may vary and there may be some difference in the candidate's answers and model answer.
6) In case of some questions credit may be given by judgment on part of examiner of relevant answer based on candidate's understanding.
7) For programming language papers, credit may be given to any other program based on Equivalent concept.

**Marks**

**1. a) Attempt any SIX of the following:** **12**

**(i) State any two mother board selection criteria.**
***(Any 2 criteria - 1 mark each)***

**Ans:**

1. Motherboard Chipset
2. Processor
3. Processor Sockets
4. Motherboard Speed
5. Cache Memory
6. SIMM/DIMM/RIMM memory
7. Bus Type
8. Basic Input Output System (BIOS)
9. Form Factor
10. Built-in Interfaces

11. On-board IDE interfaces
12. Power Management

**(ii) What is track and sector of H.D.D.?**
***(Track - 1 mark; Sector - 1 mark)***

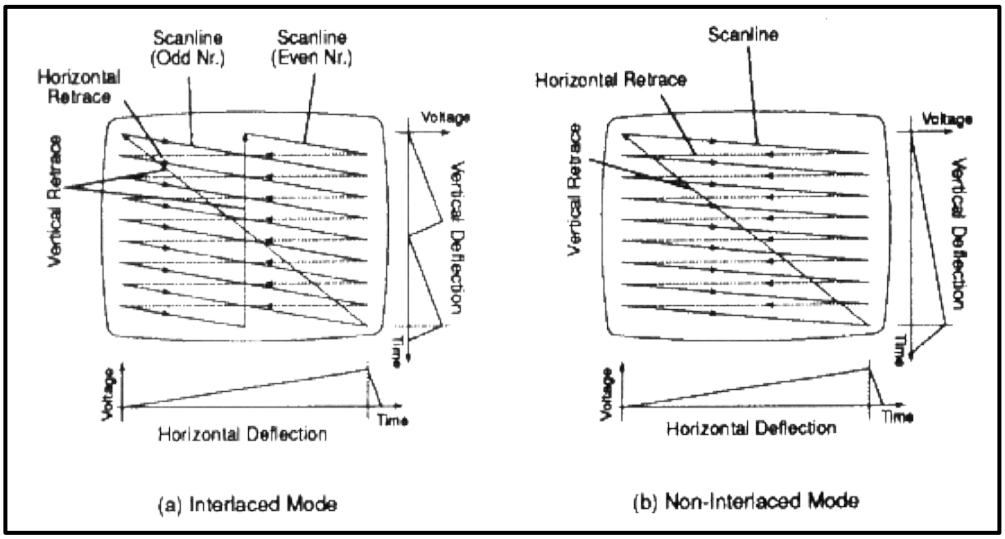
**Ans:**

**Track: -** The platters inside a hard drive are structured to facilitate the storage and retrieval of data. Each platter is divided into concentric rings called "Tracks".

**Sector:** - Each track is divided into sectors. A sector, as a rule, holds 512 bytes of data; this is usually the minimum quantity of information which is independently addressable for storage on a hard drive disk.

**(iii) What is meant by interlaced and non-interlaced monitor?**
***(Interlaced - 1 mark; Non-interlaced - 1 mark; diagram is optional)***

**Ans:**




**Interlaced Monitor:** -An interlace monitor draws an image as two passes. Once the first pass is complete a second pass fills in the rest of the image. In order to avoid a flickering image, some adapters force the monitor to create an interlaced image. Instead of the electron gun scanning from top to bottom in a continuous manner, on the first pass it will skip every next line. On the second

pass, it will scan the lines that it skipped during the first pass, thus creating full image in two scans instead of one.

**Non-Interlaced Monitor: -**

A non-interlaced monitor draws all of the lines that compose an image in one pass. The entire image is first refreshed at the vertical scanning frequency. The effective image refresh rate is only half the stated vertical scanning rate.

**(iv) Define the terms TWAIN and OCR with reference to scanner.**

***(TWAIN - 1 mark; OCR - 1 mark)***

**Ans:**

**TWAIN:**

TWAIN is a universal software interface drive that acts as an interpreter between the scanner and any TWAIN complaint application, such as a graphics program with a scanning capability. It supports multiple platform and devices. The ability to acquire images directly from the scanner is a function of the TWAIN driver.

**OCR:**

Optical Character Recognition (OCR) software works with the scanner to convert printed characters into digital text, which allows operations such as search or edit the document in a word processing program.

**(v) Give classification of printer with examples.**

***(Classification - 1 mark; Example - 1 mark)***

**Ans:**

Printers can be classified based on physical contact with the paper/surface.

**a) Impact Printer: -** Makes physical contact with the paper/surface

Examples are as follows.

(a) Dot Matrix
(b) Drum Printer
(c) Daisy wheel Printer
(d) Chain Printer

**b) Non-Impact Printer: -** Does not make physical contact with the paper/surface

Examples are as follows.

(a) Laser Printer
(b) Ink Jet Printer
(c) Deskjet printer

**(vi) Define:**

**(1) Blackout**

**(2) Surge**

***(Blackout - 1 mark; Surge - 1 mark)***

**Ans:**

**(a) Blackout**

It is the complete loss of electrical power where voltage and current drop to a very low value (typically zero). They are caused due to physical interruption in the local network.

**(b) Surge**

They are small over voltage conditions that take place over relatively long periods of few milliseconds.

**(vii) State four features of bluetooth.**

***(Any four features - ½ mark each feature)***

**Ans:**

1. It can transfer information wirelessly form one enabled device to another.
2. Bluetooth operates in the range of 2400–2483.5 MHz
3. Bluetooth uses a radio technology called frequency-hopping spread spectrum
4. Bluetooth is a packet-based protocol with a master-slave structure.
5. One master may communicate with up to seven slaves in a piconet; all devices share the master's clock.

**(viii) Give any four features of SCSI-3.**

***(Any four features; ½ mark each feature)***

**Ans:**

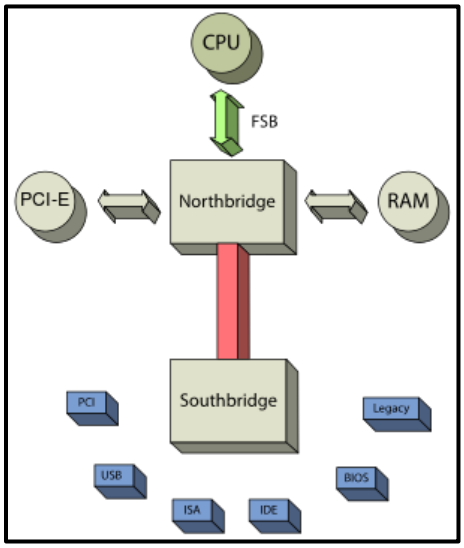
Small Computer System Interface 3 (SCSI-3) is an ongoing standardization effort for extending the features of SCSI-2. The key features of SCSI-3 include the following:

1. Additional devices on a bus (as many as 32)
2. Increased distances between devices (longer cables)
3. More command sets and device classes
4. Structured protocol model
5. Structured documentation
6. To permit backward compatibility and increased flexibility, SCSI-3 permits the use of many different transport systems, some parallel and some serial. For every transport, the command set and software protocol are the same.
7. **Fast-80(DT) Data Transfer:** Reflecting the continuing appetite for speed on the SCSI bus, data transfer rates were again doubled, this time to 160 MB/s on a wide bus. This was accomplished not by increasing the speed of the bus from 40 MHz to 80 MHz, but rather through the use of double transition clocking; thus the "DT" sometimes found in the name for this signalling speed.
8. **Cyclic Redundancy Check (CRC):** This is a common error checking protocol used to ensure data integrity. It was added as a safety measure since transfer speeds were being increased, leading to the possibility of data corruption.
9. **Domain Validation:** This feature improves the robustness of the process by which different SCSI devices determine an optimal data transfer rate;
10. **Quick Arbitration and Selection (QAS):** This feature represents a change in the way devices determine which has control of the SCSI bus, providing a small improvement in performance.
11. **Packetization:** Another small change to improve performance, packetization reduces the overhead associated with each data transfer;

**b) Attempt any TWO of the following:** **Marks 8**

**(i) Draw block diagram of north bridge / south bridge architecture and explain.**
***(Diagram - 2 marks; Description - 2 marks)***

**Ans:**




Intel's earlier chipset were broken into multi-tired architecture known as North Bridge and South Bridge components as well as Super I/O chip.

**North Bridge:** It is the connection between the high speed processor bus and the slower AGP & PCI buses. Northbridge is also referred to as PAC (PCI-AGP) controller is the main component of the motherboard and only motherboard circuit (besides the processor) that runs at the full motherboard speed. It serves as the four way connection between CPU, Memory, Video card and south bridge.

**South Bridge:** It is the bridge between PCI bus and even slower ISA bus. Super I/O chip: contains commonly used peripheral items all combined in single chip. The Southbridge is the lower speed component of the chipset. The south bridge connects to the 33MHz PC and contains the interface to ISA bus. It also contains dual ATA/IDE hard disk controller interfaces, one or more USB interfaces, CMOS RAM, real time clock functions, interrupt controller, DMA controller. Super I/O chip contains serial port, floppy controller, keyboard & mouse interface.

**(ii) Describe passive matrix and active matrix with suitable diagrams.**
***(Passive Matrix - 2 marks; Active Matrix - 2 marks)***

**Ans:**

**Passive matrix LCD**

Passive matrix LCDs use a simple grid to supply the charge to a particular pixel on the display. The liquid crystal material is sandwiched between the two glass substratesand a polarizing film is added to the outer side of each substrate. To turn on a pixel, the integrated circuit sends a charge down the correct column of one substrate and a ground activated on the correct row of the other.

The row and column intersect at the designated pixel, and that delivers the voltage to untwist the liquid crystals at that pixel.

To address a pixel the column containing the pixel is sent a charge, the corresponding row is connected to ground. When sufficient voltage is placed across the pixel, the liquid crystal molecules align parallel to the electric field.

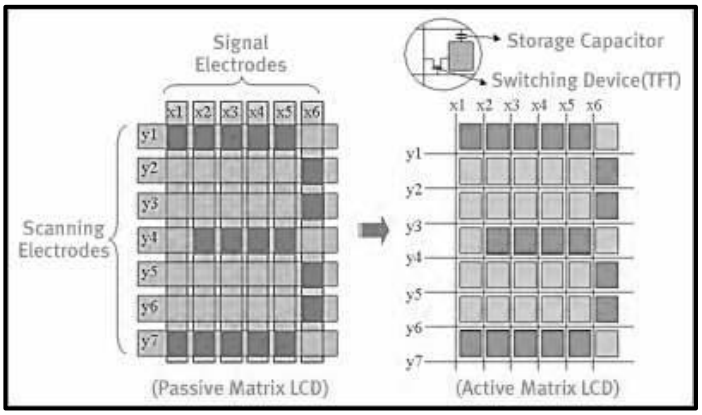
In passive matrix LCDs (PMLCDs)there are no switching devices, and each pixel is addressed for more than one frame time.

**Active matrix LCD**

In active matrix LCDs, a switching device and a storage capacitor are integrated at the each cross point of the electrodes.

The active addressing removes the multiplexing limitations by incorporating an active switching element.

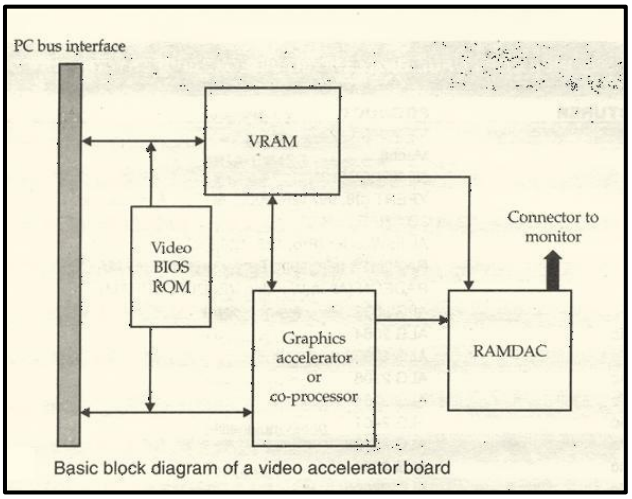
In contrast to passive matrix LCDs, active matrix LCDs have no inherent limitation in the number of scan lines, and they present fewer cross talk issues.



**(iii) Draw the block diagram of a video accelerator card and explain.**

***(Diagram - 2 marks; Description - 2 marks)***

**Ans:**



Basic block diagram of a video accelerator board

The core of the accelerator is the graphics chip (or Video chipset). The graphics chip connects directly with the PC expansion bus. Graphics command and data are transmitted into pixel data and stored in Video memory. It offers a second data bus that is routed directly to the Video board's RAM DAC (Random Access Memory Video to Analog Converter). The graphics chip directs RAM DAC operation and ensures that VRAM data is available. The RAM DAC then translates Video data into Red, Green and Blue video signals along with horizontal and vertical synchronization signals, which are the output signals generated by the monitor. This architecture may appear simple, but this is due to high level of integration provided by the chipsets being used.

**2. Attempt any <u>FOUR</u> of the following: 16**

**a) Explain four features of PCI bus.**

***(Any 4 Features - 1 mark each feature)***

**Ans:**

1. **Plug and Play: -** Just connect device and use it.
2. **Hot plug-ability: -**Devices can be connected while system is running.
3. **Hot swappable: -** Flexibility in removing or replace device with another device without significant interruption to the system.

4. **New Approach: -**PCI is latest approach as compare to earlier bus.
5. **High speed: -** 32 bits and 64 bits enable PCI to transfer data at high speed.
6. **Backward compatibility: -** Older versions of independent bus can be connected to PCI Slot.
7. **Independent bus: -** Device operates independently without CPU intervention.
8. **High operational frequency:-** Operates at frequency up to 133MHz.

**b) List four recording techniques used in storage devices and explain any one.**
***(List - 2 marks; Description of any 1 technique - 2 marks)***

**Ans:**

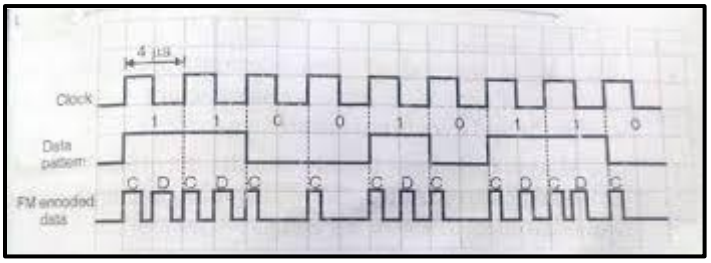
- FM (Frequency Modulation)
- MFM(Modified Frequency Modulation)
- RLL (Run Length Limited).
- Perpendicular Recording

**FM ENCODING**

The FM method of encoding digital data onto a disk uses two pulse periods to represent each bit of data (a pulse period is the time span of one pulse). The first pulse period always contains a clock pulse. The second pulse-period may, or may not, contain a data pulse. If the digital data is a "1," a data pulse will be present in the second pulse-period.

But, if the digital data is a "0," then there's no pulse present.

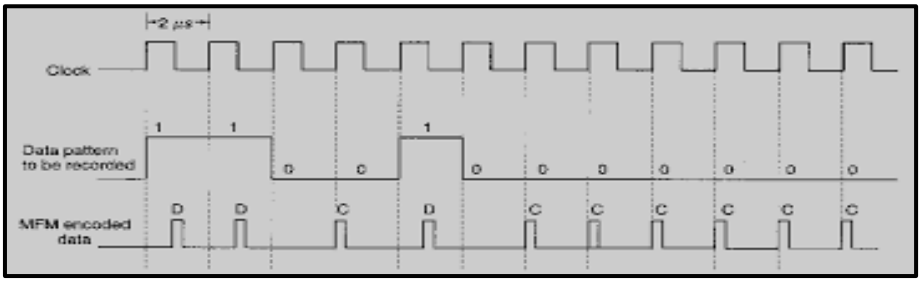
The clock pulse, which is always present, tells the disk drive's interface that the next pulse is a data pulse. It is used to compensate for changes in the disk's rotation speed.




**MFM Encoding Scheme:**

More data can be stored on the same surface or the data storage density can be increased, if the number of pulses required to store the data can be minimized. When minimizing the pulses, one should be careful that the number of no pulses together should not be very long; otherwise the disk controller may go out of synchronization with the data.

The MFM (modified frequency modulation) method of data storage, by reducing the number of pulses, is able to store more data without any data and synchronization number of pulses, is able to store more data without any data and synchronization loss.
In MFM recording the 0s and 1s are encoded as given below
1 is always stored as no pulse, and a pulse (NP)
0, when preceded by another 0, is stored as a pulse, and no pulse(PN)
0, when preceded by a 1, is stored as two no pulses(NN)
If you store 1001 on the disk surface using the MFM storage method, it would be store das NP NN PN NP.




**RLL Encoding Scheme**
The RLL is encoding or the Run Length Limited encoding is the most common encoding scheme used in the hard disk storage. This encoding scheme can be more accurately called as 2,7 RLL encoding because in this scheme in a series or in a running length the minimum number of 0s next to each other is two, and the maximum number of 0s together cannot be more than seven.
The RLL encoding scheme can store 50 percent more information than MFM encoding scheme on a given surface and it can store three times as much information as the FM encoding scheme.
The Run length Limited name comes from the minimum number (run Length) and maximum number (run Limit) of "no pulse" values allowed between two pulses.
For the RLL encoding, an encoder/decoder (Endec) table is used to find the pulse signal to be used for different data bit groups. Endec table used by the IBM to convert bit information to the pulse signal is shown below

| Data Bit | Pulse Encoding |
|---|---|
| 10 | NPNN |
| 11 | PNNN |
| 000 | NNNPNN |
| 010 | PNNPNN |
| 011 | NNPNNN |
| 0010 | NNPNNPNN |
| 0011 | NNNNPNNN |

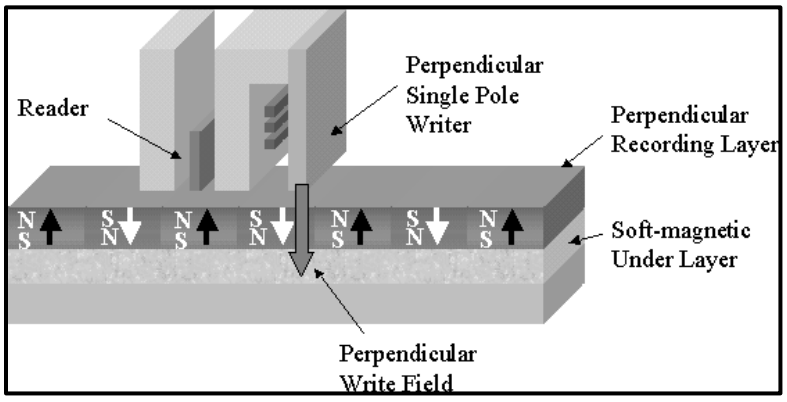
**Perpendicular Recording Scheme**

All hard disk drives (HDD) use magnetic media to record data using longitudinal recording (FM, MFM, RLL) which stores magnetic bit horizontally across the surface of the medium.

However, perpendicular recording which aligns magnetic signals perpendicular on media has the potential to achieve higher data density because of vertically oriented magnetic bits.

The recording head for perpendicular recording consists of a single pole inductive write head with the suitable flux return path designed for high efficiency, low stray field sensitivity and sharp field gradient capable of writing on perpendicular media.

They use less space than longitudinal space bits. With perpendicular recording technology hard disk drive storage capacity can be increased.



**c) What is partitioning of hard disk? How it is done? Give need of partitioning.**
***(Definition - 2 marks; procedure - 1 mark; need - 1 mark )***

**Ans:**

**Definition:-**

Partitioning is a procedure which divides the hard disk into multiple sections or logical parts or drives. Each partition is comprised of several cylinders or tracks.

**Procedure to create partition: -**

***Method 1:***

1.Use fdisk.exe command prompt utility to create partitions.

***Method 2:***

1. Run diskmgmt.msc utility.
2. Select volume which is to be partitioned in small/logical volume.
3. Right click and select shrink volume option.
4. Set Size and Assign Drive name.
5. Format new drive with appropriate file system.

**Need of partitioning:-**

1. Different operating systems may be stored on different partitions.
2. To segregate data as per user choice.
3. To create separate memory space for back up.
4. Maximize Hard disk utilization.

**d) Describe use of jumper selection. (any four)**
***(Any 4 use of jumper select - 1 mark each)***

**Ans:**

1. Jumpers allow the computer to close an electrical circuit, allowing the electricity to flow certain sections of the circuit board.
2. Jumpers are used to configure the settings for computer peripherals such as the motherboard, hard drives.
3. If motherboard supports intrusion detection, a jumper can be set to enable or disable this feature.
4. Before Plug-and-Play, jumpers were used to adjust device resources, such as changing what IRQ the device is using.

**Common setting configuration protocols are used for hard disk drives:**

**Single**: the hard drive is the only device on the IDE interface cable.

**Master/Slave:** the hard drive is either a Master (C:/) drive or a Slave drive in a multiple-drive system.

**Cable Select (CSEL/CS):** jumper settings are the same on all hard drives in a system (both single- and multiple-drive systems); however, a special CSEL cable must be used, and the host system must support CSEL. WD EIDE hard drives are factory set for Cable Select configuration.

**Limit:** Limit data transfer rate to 1.5Gbits per second.

**e) Write advantage and disadvantage of LCD monitor.**

***(Any 2 Advantages - 2 marks; Any 2 Disadvantages - 2 marks)***

**Ans:**

**Advantages of LCD:**

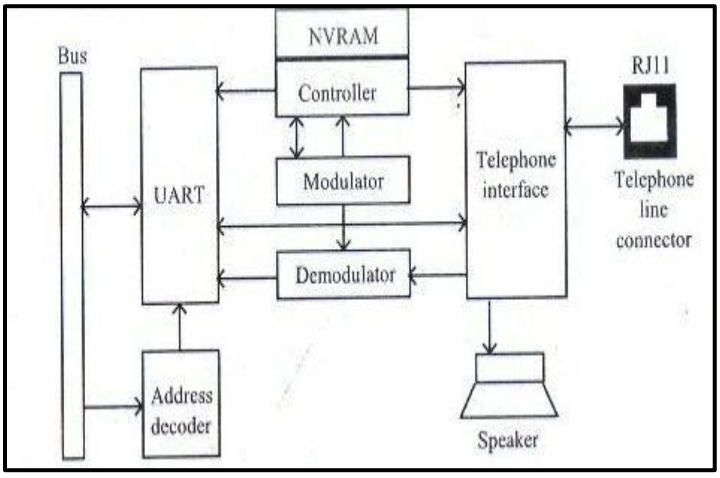
- LCD monitors consume less power. An average 19-inch LCD uses 45 watts of electricity, while a 19- inch CRT uses 100 watts.
- LCD monitors are smaller, thinner and weigh half as much as CRTs.
- An LCD monitor's tilt, swivel, height and orientation from horizontal to vertical can all be adjusted easily.
- LCD monitors don't produce the flicker that CRTs do, generating less eye strain
- Light weight; can be about 15 lbs for a thin LCD. Smaller footprint on desk leaving, freeing up the work area on the user's desk.
- Low frequency radiation is practically eliminated
- Energy efficient, they do not generate heat.
- Potentially less eyestrain due to reduced screen glare.

**Disadvantages of LCD:**

- Designed only for one optimum resolution; cannot adjust images.
- There can be pixel defects in LCD panels.
- LCD has smaller viewing angle and at larger viewing angle the image quality is poor.
- The colour reproduction is poor in LCD.

**f) Draw block diagram of internal modem and state the function of various blocks.**
***(Diagram -2 marks; Description -2 marks)***

**Ans:**




It contains its own Universal Asynchronous Receiver/Transmitter (UART).
A modulator Circuit converts the serial data from the computer into audio signals to be transmitted over telephone lines. This modulated audio is then coupled to the telephone line. The signal passes through telephone jack (RJ 11) connector at the rate of the modem to the telephone line.
On the receiver side, signals received from the telephone line must be translated into serial data. The telephone interface separates the received signals and passes them to the demodulator. After demodulation the resulting serial data is passed to UART, which in turn converts the serial bits into parallel words that are placed on the system's data bus.
The telephone interface also generates Dual Tone multi Frequency (DTFM) dialling signals needed to reach a remote modem. When the remote modem dials in, the telephone interface detects the incoming signal and alerts the UART to begin negotiating a connection.
The telephone interface drives a speaker. During the initial stages of modem operation the speaker is used to hear the dial tone, dialling signals, and audio negotiation between the two modems. Once the connection is established, the speaker is disabled.
The controller circuit manages the overall operation of the modem. It switches the modem between the control and data operating modes. The controller accepts commands from the modulator that allow the modem characteristics and operating parameters to be changed.

**3. Attempt any FOUR of the following**: **16**

**a) State different functions of BIOS.**
***(Any four Functions - 1 mark each)***

**Ans:**

The BIOS (Basic Input Output System) provides the processor with the information required to boot the system from a non-volatile storage unit (HDD, FDD, CD or other). It provides the system with the settings and resources that are available on the system

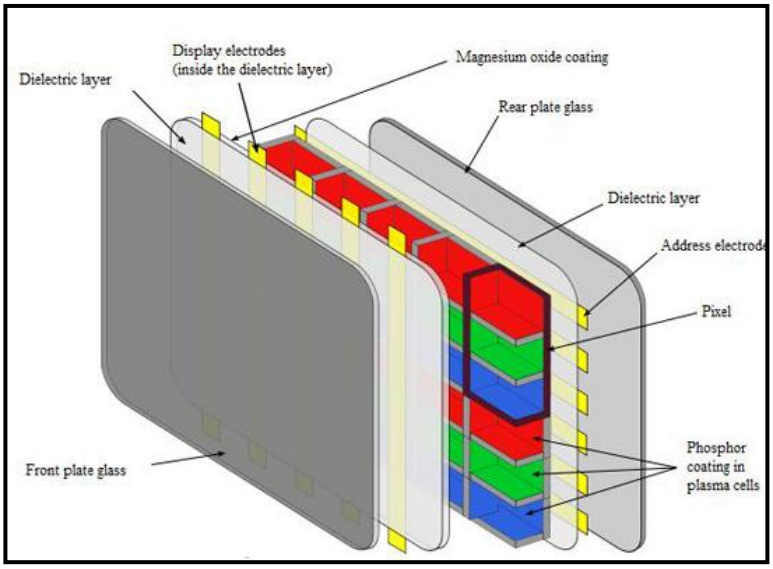
**Main functions of BIOS**

1. The main function of the BIOS is to give instructions for the power-on-self-test (POST). This self-test ensures that the computer has all of the necessary parts and functionality needed to successfully start itself, such as use of memory, a keyboard and other parts.
2. If errors are detected during the test, the BIOS instruct the computer to give a code that reveals the problem. Error codes are typically a series of beeps heard shortly after startup.
3. The BIOS also works to give the computer basic information about how to interact with some critical components such as drives and memory that it will need to load the operating system.
4. Once the basic instructions have been loaded and the self-test has been passed, the computer can proceed with loading the operating system from one of the attached drives.
5. Computer users can often make certain adjustments to the BIOS through a configuration screen on the computer. The setup screen is typically accessed with a special key sequence during the first moments of the startup. This setup screen often allows users to change the order in which drives are accessed during startup and control the functionality of a number of critical devices. Features vary among individual BIOS versions.
6. Many PC manufacturers today use flash memory cards to hold BIOS information. This allows users to update the BIOS version on computers after a vendor releases an update. This system was designed to solve problems with the original BIOS or to add new functionality.

**b) Explain working and construction of plasma display technology.**
***(Working - 2 marks; Construction - 2 marks)***

**Ans*:***

**Plasma Display**

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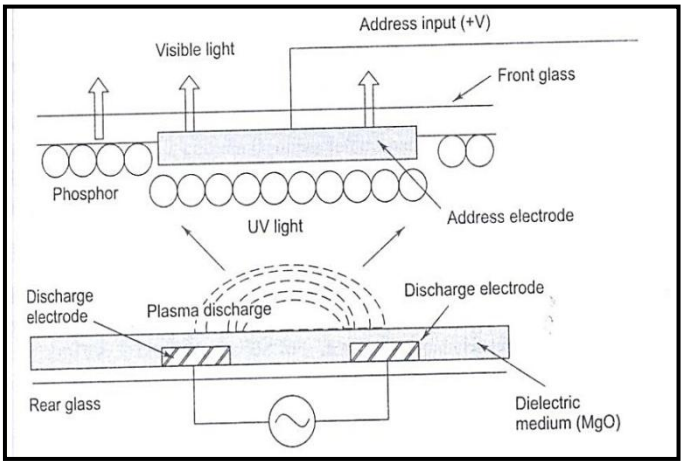



Plasma is a slate of gas made up of free flowing ions (+ve) and electrons. Under normal conditions a gas is made up of uncharged particles.

**Construction:**

1. Xenon and Neon Gas
2. Address Electrodes
3. Display/Discharge Electrodes
4. Dielectric Medium (MgO Magnesium Oxide)
5. Phosphor (Red, Green and Blue Triad)

**Working:**

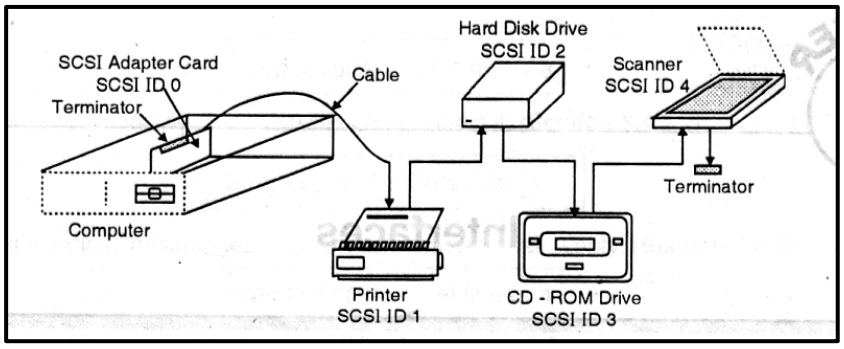
- In plasma display xenon and neon atoms are used.
- When an electric current is passed through plasma, the electrons rush towards the positive electrode and ions rush towards the negative electrode.
- During this rush they collide with each other. These collisions excite the gas atoms in the plasma, causing them to release photons of energy.
- These are ultraviolet photons invisible to human eye.
- The released ultraviolet photons interact with phosphor material on the inside wall of the cell and phosphors give off colored light.
- Each phosphor has three separate cells, a red, a blue and a green phosphor.
- These colors blend together to create the overall color of the cell.
- The xenon and neon gas in plasma contain hundreds of thousands of tiny cells positioned between two plates of glass.
- Long electrodes are sandwiched between the glass plates on both the sides of the cells.
- The address electrodes are at the rear glass plate and the discharge electrodes are transparent and mounted along the front glass plate.
- Both sets of electrodes extend across the entire screen.
- To ionize the gas in a particular cell, the electrodes that intersect at that cell are charged.
- When an electric current flows through the gas in the cell, the gas atoms are stimulated and they release ultraviolet photons.
- By varying the pulses of current flowing through the different cells intensity of each sub-pixel color can be varied to create hundreds of different combinations of red, green and blue.

**c) Explain in brief SCSI drive configuration.**
***(Explanation - 4 marks; Diagram - optional)***

**Ans:**

**SCSI** (**Small Computer System Interface**) pronounced as **scuzzy**
SCSI (Small Computer System Interface) is a set of standards for physically connecting and **SCSI** (**Small Computer System Interface**) pronounced as **skuzzy**

1. SCSI device Id: Every device on a SCSI bus must be uniquely identified for addressing purposes. Jumpers can be used for assigning ID number
2. Termination Activate: The devices on the end of the SCSI bus must terminate the bus. If HDD is the end, then if the jumper is set, it terminates properly. All drives do not support termination
3. Disable Auto start: This jumper will not allow the drive to start till it gets the start signal. It avoids loading the P/S
4. Delay Auto start: The jumper indicates that the drive start automatically but allows a few seconds for power to be applied
5. Stagger spin: When a system has multiple HDD, no two drives on the same SCSI channel will start simultaneously
6. Narrow/ wide: Some drives have jumpers to control whether they will function in narrow or wide mode
7. Disable Parity: Turns off parity checking on the SCSI bus for compatibility with host adapters that do not support that feature.



**d) Explain the working of logic analyzer for troubleshooting of PC with neat diagram**
***(Diagram - 2 marks ; Explanation - 2 marks)***

**Ans:**

**Logic Analyzer:**

- A logic analyzer is an electronic instrument that displays signals in a digital circuit that are too fast to be observed and presents it to a user so that the user can more easily check correct operation of the digital system.

Fig. shows functional block diagram of logic analyzer. A logic analyzer is a device, which allows you to see the signals on 16 to 64 signal lines at once. It is also called multi-trace digital oscilloscope.

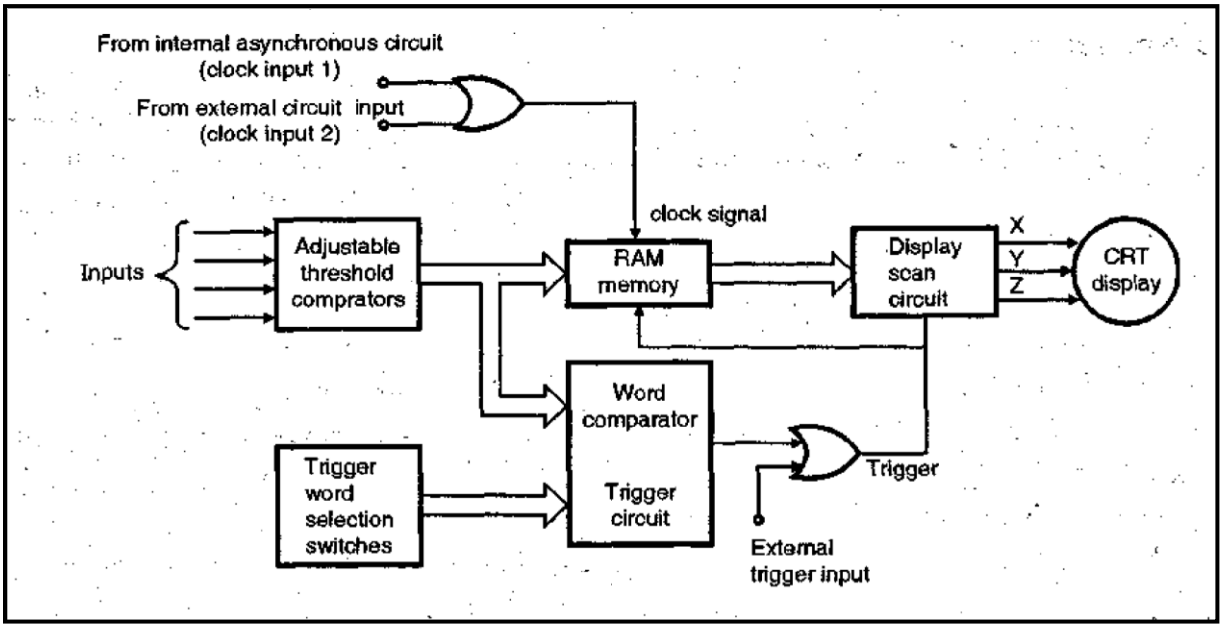



**Fig. Block diagram of logic analyzer**

It captures and stores several digital signals, letting you view the signals simultaneously

**Working:**

- All the input signals are applied to the adjustable threshold comparator one for each channel.
- Then reference input for each signal can be adjustable depending on logical state of device under testing.

- The logic analyzer takes sample of each input signal from comparator whenever clock signal is applied to memory and to stores into memory.

- The clock input may be from :

  - **Internal asynchronous clock input:** It produced by internal oscillator, which is very stable in operation.

  - **External clock input:** It is clock from any external source. It takes around 256 to 1024 samples of each signal and stores them in memory.

- When trigger is applied to memory, memory displays these stared samples.

- The trigger input may be from Word comparator or External trigger input.

  - The word comparator generates trigger when it's two input one from adjustable threshold comparator and another from word selection switch. If both inputs code are same then it send trigger to memory.

- After applying trigger to memory, then it send to display scan circuit.

The display scan circuit then constructs the original waveform and displays it on the CRT

**e) Give the test sequence of POST.**

***(Correct Sequence - 4 marks; Description - Optional)***

**Ans:**

1. **CPU Test**
   Different flags and registers within the CPU are tested. Testing is done by setting, resetting and moving the data from one register to another. If the any flag is not reset then system is halted with the execution of the halt instruction. On noticing any error system is halted.
2. **BIOS ROM Test**
   The contents of the 8k ROM containing POST and BIOS is verified by checksum calculation method. The subroutine for ROM checksum performs EXOR addition of the content of all the locations in the 8K ROM from the start address, and if checksum result is zero, then the content of the ROM are OK. The last location contains the checksum of the previous locations and if the checksum is not zero then system is halted with the execution of the halt instruction. If BIOS is corrupted or IPL has Fault, when such error's are detected, the CPU is halted and the checkpoint 01 is present on port A pins.

3. **Timer 1 Test**
   The timer 1 in PIT (8253) is tested. The Timer 1 is set as rate generator in mode 2 .Set an initial value in Timer 1 .Latch. Timer 1 count .After some delay read Timer1 count and check if it counts too slow. If so, the POST halts. When Timer is reset, a mild click sound is heard from the speaker on detecting an error, the CPU is halted and checkpoint 02 is present on port a pins.
4. **DMA Channel 0 Test**
   The channel 0 of DMA controller is tested here. In this portion of POST, the channel 0 of DMA controller is initialized with appropriate start address and byte count values, so that this channel is ready for performing memory refresh DMA cycles when Timer 1 sends DMA Request signal The CPU is halted if any error is found and checkpoint 03 is present on port A pins.
5. **Base 16K RAM Test**
   The first 16 k RAM occupying the address hex 00000 to 03FFF is tested. In each location five different test patterns (00, FF, 55, AA, 01) are written and verified by reading back. There are two types of failures during this test:

(a) The pattern written and the pattern read are different
(b) The pattern written and the pattern read may be same but there is parity error during reading. If any error is noticed, check point 04 and failing bit pattern are alternatively outputted repeatedly on port A pins. During warm boot, the POST skips the video RAM test.

6. **CRT Controller Test**
   CRT controller 6845 and the video buffer RAM in the display adapter are tested. Display adapters can be configured by setting the DIP switches which post identifies by reading DIP switch If no display adapter is present, the POST skips all video adapter tests If any error is noticed, beep sounds are produced on the speaker.

7. **Motherboard Support Chips Test**
   The interrupt controller, timer (8253) **and** keyboard interface are tested here. If any error is noticed, an error code is displayed on the CRT monitor.

8. **RAM Test**
   RAM after the first 16 kb is tested here for five different patterns (AA, 55, FF, 01 and 00). A detailed error message indicating the failing address and failing bits is displayed on the CRT screen.
9. **Optional ROM Test**
   The ROMs in hard disk controller are tested by checksum method.

10. **Peripheral Controller Test**
    The Floppy Controller, Parallel Ports, Serial Ports and Hard Disk Controller are tested here. A detailed error message is displayed on the screen if any error is noticed.

At the end of all the tests, the POST passes control to the boot strap loader program in BIOS. The boot strap loader reads the initial program from track 0 on floppy disk or hard disk. This initial program reads more programs from the floppy disk or hard disk, which is nothing but the DOS.

**f) Which different testing are performed by diagnostic software?**
***(Explanation - 4 marks)***

**Ans:**

The PC has a sophisticated hardware fault which is not detected by POST. There are problem in the system but it is not known whether it is hardware or software problem.

1. Sophisticated hardware faults
   Diagnostic software can test and detect problems on all motherboard components, drives, ports, and slots Diagnostic software perform,

- CPU testing
- hard drives testing
- SSDs testing
- RAM testing
- optical drives (CD, DVD and Blu-ray) testing
- sound cards testing
- graphics cards testing (GPGPU, Video RAM, 2D graphics, 3D graphics and video playback)
- network ports testing
- printers testing
- microphones testing
- webcams testing
- battery's testing
- tape drives testing
- USB ports (USB 3.0 and 2.0) testing
- Serial ports and Parallel ports testing

2. Hardware – Software problem isolation

- Certain problem caused by errors in the system software or application program may appear to be hardware or software faults.
- In such cases If the diagnostic program run successfully, it will isolate the problem easily i.e. hardware or software problem.

3. Intermittent hardware fault

- If there is any intermittent hardware fault in the PC, it may not be caught by POST, even diagnostic program may run successfully once or twice.
- But when you repeatedly and continuously run the diagnostic program for long time then intermittent hardware fault will be caught.

**Marks**

**4. Attempt any FOUR of the following: 16**

**a) With neat diagram explain the working of optical mouse.**
***(Diagram - 2 marks ; Explanation - 2 marks)***

**Ans:**

1. In this type of mouse, instead of the customary ball and rollers, a light source and photo-detector is used with a special mouse pad.
2. When the optical mouse is moved on this special pad, light from the light source gets reflected from the pad and special photo-detectors inside the mouse detect the horizontal and vertical movement based on the reflected light received.
3. One of these photo-detector is used to detect the back-and-forth movement of the mouse, i.e., vertical movement of the cursor on the screen and the other photo-detector is used to detect the side-to-side movement of the mouse, i.e., the horizontal (left to right and right to left) movement of the cursor on the screen.
4. The movement of the cursor on the screen depends on the number of the signals that is passed to the PC through the wire connected with the mouse.
5. The PC in turn, passes them to the mouse driver software which then converts them into distance, direction and speed required for the movement of the screen cursor.
6. Depressing any of the mouse button also produces a signal which is passed to the PC and the PC passes it to the software.
7. Depending upon the button being pressed, number of times the button being pressed and the present location of the cursor on the screen, the software accomplishes the task desired by the user.

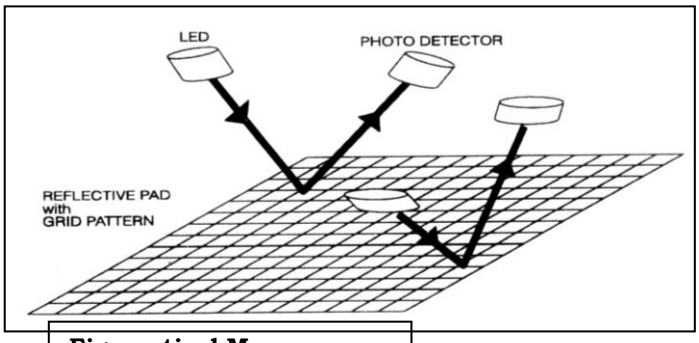
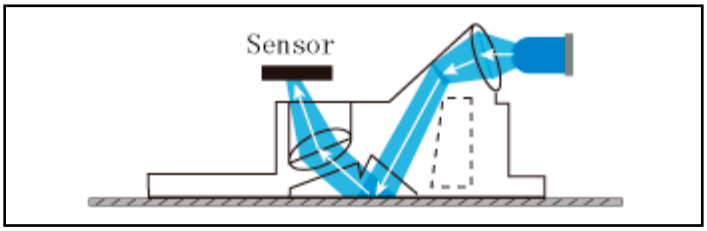



**Fig : optical Mouse**

**OR**



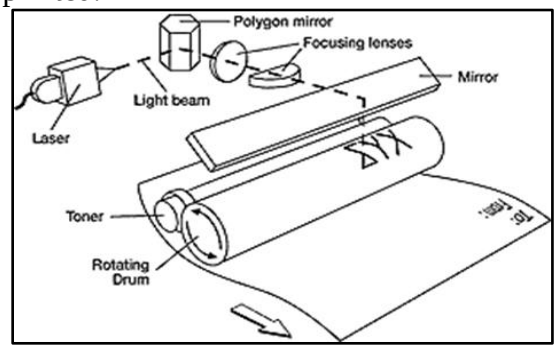

**b) Explain in brief working of laser printer with neat diagram.**
***(Any Diagram - 2 marks; Explanation - 2 marks)***

**Ans:**

**Working of Laser Printer:**

- The laser printing process starts with the transmission of the data from the computer or data storage device to the printer's image processor.
- The image processor rasterizes the data and converts the information received into a graphic image; this image is then sent to the printer's memory in preparation for 'transmission'.
- Meanwhile, the photosensitive drum revolves and touches the charged roller or the charged corona wire. The wire or the roller imparts its negative charge to the drum and as a result the latter acquires a negative static charge.
- This static charge remains on the drum's surface as long as it's dark. At this point, the laser assembly emits a light beam onto the revolving photocell.
- The laser beam passes through a series of focusing mirrors so that it would hit the drum precisely.
- This laser beam is activated and triggered by the data stored in the image processor memory.
- At the points of the drum hit by the laser beam, the charge is reversed from negative to positive.
- Through this process, the image is outlined and drawn on the drum by the laser beam; that is, the positively-charged portions of the revolving drum or photocell represent the complete image of the text or picture to be printed.
- Now, the drum or the photocell touches the negatively charged toner.
- This toner clings to all the positively charged portions of the photocell and leaves all the negatively charged portions alone.
- At this point, the photocell bears the actual image.
- Next, the photocell or the drum rolls over the paper and the toner is transferred to the latter.
- The paper with toner then passes through the fuser assembly which bonds the toner particles to the paper.

- Through a combination of heat (coming from a heat source within the fuser's tube) and pressure, the toner powder (made of wax or other easy to melt substance) melts on and gets bonded with the paper.
- The paper then comes out printed.

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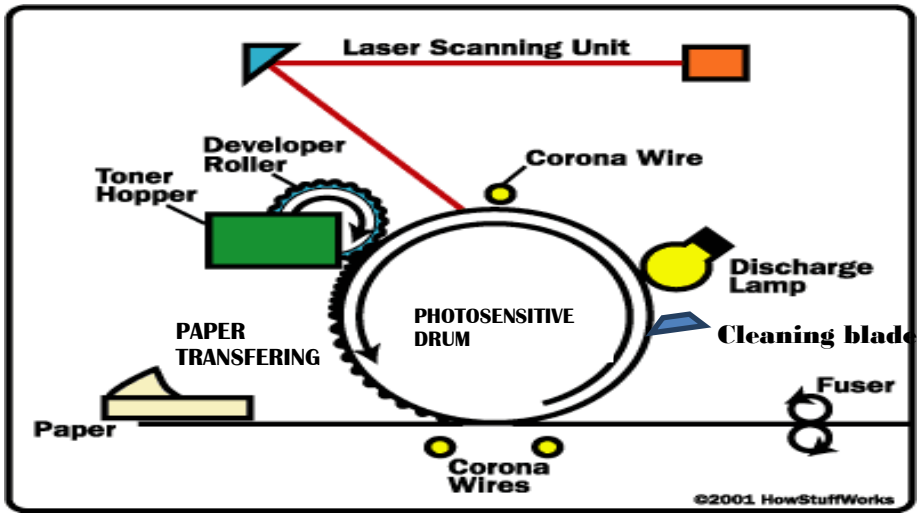


**c) Write difference between on-line UPS and off-line UPS.**
***(Any four; Each Point – 1 mark)***

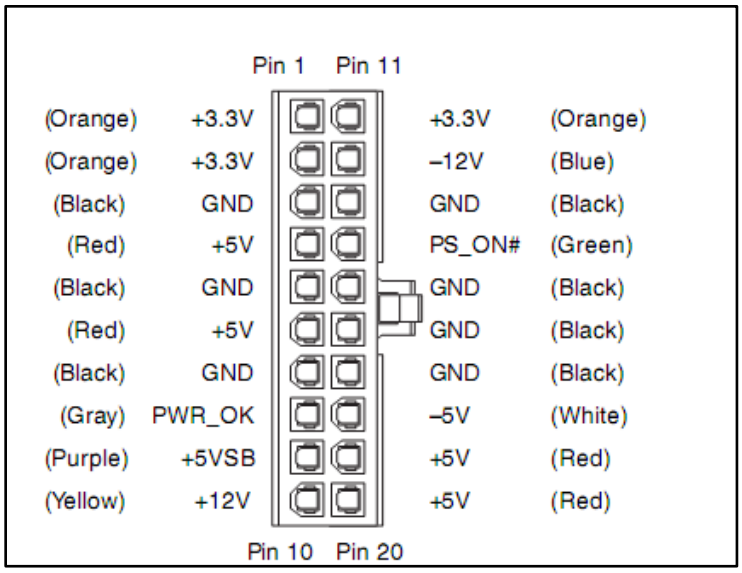
**Ans:**

**Off-line UPS:**

| On-Line UPS | Off-Line UPS |
|---|---|
| Battery is continuously charged and then delivers DC power to inverter for converting to AC and supplying to the PC | Battery is charged when AC mains are on and as soon as AC mains are off, battery discharges and supplies power to the PC. |
| Switching is not involved | Switching is involved |
| It is at high speed so as to avoid resetting of PC. | It is not at high speed, therefore resetting may occur some times. |
| Spikes are not generated | Spikes are generated. |
| On-line UPS's are the complex and expensive. | Offline UPS's are the simplest and least expensive |
| Online UPS can provide protection from the common power problems. | Offline UPS does not provide protection from the power problems. |

**d) Draw pinout diagram and signal description of ATX connector**
***(Diagram -2 marks; Explanation -2 marks)***

**Ans:**




- The ATX/NLX provides 5 DC voltages +5V,-5V,+12 V, -12 V and +3.3 V through a 20-pin connector.
- PS-ON: The PS-ON is an input from motherboard to SMPS only when this signal is low, the SMPS outputs should be ON. Otherwise the output should be OFF. The signal can be generated by software
- 5 VSB: The 5 VSB is a standby voltage which supplies power to special circuits even when the SMPS and the System are off.
- PW-OK: The PW-OK is a power good signal (PGS) indicated during the booting process.

**e) Write features of fire wire. (any four)**
***(Any four; Each Point - 1 mark)***

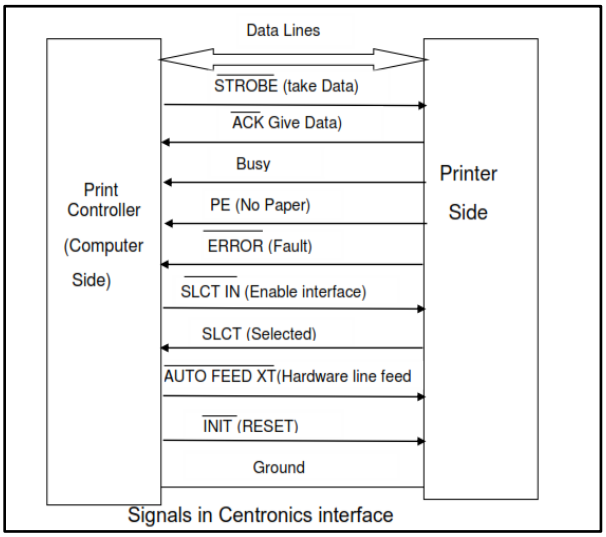
**Ans:**

- Hot pluggability.
- Fire wire can connect together up to 63 peripherals in a cyclic topology.
- Uses daisy chain topology
- Data Transfer Rate 400/ 800 Mbps
- Has a 6-pin connector, for Power, Ground and 2 twisted pair cables for Send and Receive.
- Snap connection: no need for device ID, jumper, DIP switch, terminators etc.
- Dynamic reconfiguration.
- Max distance between devices: 4.5m
- Supports DMA transfers - It allows peer-to-peer device communication, such as communication between a scanner and a printer, to take place without using system memory or the CPU.
- Well suited for different devices such as Digital Camera, Scanner, HDD, printers, music systems
- It is designed to support plug and play and hot swapping.
- It uses six wire cable which is more flexible than most parallel SCSI cables and can supply upto 45 watts of power per port at upto 30 volts.

**f) Draw the diagram of centronics interface and explain function of any four signals.**
***(Diagram -2 marks; Explanation -2 marks)***

**Ans:**

The Centronics parallel interface is an I/O interface for connecting printers and certain other devices to computers.



Signals in Centronics interface

**Signals from PC to Printer**

There are 12 signals from the PC to the printer. Out of these 8 signals are data bits and 4signals are control signals. These are

| | |
|---|---|
| $\overline{STROBE}$ | The printer should take data when this signal is low. |
| $\overline{INIT}$ | When it is low the printer resets its electronics logic and clear the printer buffer |
| $\overline{SLCTIN}$ | It is an interface enable signal when this signal is low the printer responds to signals from the controller |
| $\overline{AUTOFEEDXT}$ | After printing every line, the printer will provide one line feed automatically if this signal is low. This type of line feed known as hardware line feed. |

**Signals from printer to PC**

There are 5 status signals from the printer to the PC. These are

| | |
|---|---|
| $\overline{ACK}$ | This Signal is an acknowledgement for $\overline{STROBE}$ Signal from PC. When active, it indicates that printer has received data sent by The PC and the printer is ready to accept next data byte |
| $BUSY$ | When BUSY Signal is high it indicates that the printer is busy and it cannot receive data. This signal becomes high under any of the four signals<br>1) On Receiving STROBE active<br>2) During printing operation<br>3) When the printer is in off line start<br>4) When the printer senses some error condition |
| PE | When PE Signal is high it indicates that there is no paper in the printer |
| $SLCT$ | $SLCT$ Signal indicates that the printer is selected and logically connected to PC |
| $\overline{ERROR}$ | This signal indicates that there is some error condition in the printer. This signal becomes active under any of the following<br>Three reason<br>1) Mechanical fault or electronic fault in the printer<br>2)The printer is in off line state<br>3)There is no paper in the printer |

**5. Attempt any TWO of the following**: **16**

**a) What is need of cache memory? Describe the types of cache memory.**
***(Need - 2 marks; internal - 3 marks; External - 3 marks)***

**Ans:**

Cache is a smaller, faster memory which stores copies of the data from the most frequently used main memory locations. When the processor needs to read from or write to a location in a main memory, it first checks whether a copy of that data is in the cache. If so, the processor immediately

reads from or writes to the cache, which is much faster than reading from or writing to the main memory. The CPU uses cache memory to store instructions that are repeatedly required to run programs, improving overall system speed. Static RAM is used as cache memory to improve the speed of computer, and Used in between main memory and processor.

**Types of Cache:**
**Internal Cache:-**
Cache built into the CPU itself is referred to as level 1 (L1) cache.
L1 or primary cache is a small high speed cache incorporated right onto the processor's chip.
The L1 cache typically ranges in size from 8KB to 64 KB and uses high speed SRAM instead of slower and cheaper DRAM used for main memory

**External Cache:-**
Cache that resides on a separate chip next to the CPU is called as level 2 (L2) cache.
L2, or secondary cache memory between the RAM and the CPU (but not on the CPU chip itself) bigger than the primary cache (typically 64KB to 2MB).
Some CPUs have both L1 and L2 cache built-in and designate cache chip as level 3(L3) cache.
L3 cache:
L3 cache is slowly replacing the L2 cache function and the extra cache built into the motherboards between the CPU and the main memory (old L2 cache definition) is now being called the L3 cache.
Some manufacturers have proprietary L3 cache designs already, but most desktops do not offer this feature yet.

**b) Describe real and protected mode of processor in detail.**
***(Real mode - 4 marks; protected mode - 4 marks)***

**Ans:**

**Real Mode:**

- It is based on 8086 & 8088 processor.
- The original IBM PC included an 8088 processor that could execute 16 bit instructions using 16 bit internal registers and could address 1 MB using 20 address lines.
- The 16 bit instruction mode of 8088 is called the real mode.
- All software running in the real mode must use only 16 bit instructions and work within 20 bit memory architecture it supports.
- No multi tasking – no protection is there to keep one program from overwriting another program
- All processor have real mode available and in fact the computer normally stat up in real mode.
- Real mode is used by DOS and Standard DOS applications.

**Protected Mode:**

- Starting with the 80286 chip in the IBM AT, a new processor mode was introduced called protected mode. This is a much more powerful mode of operation than real mode, and is used in all modern multitasking operating systems.
- Full access to all of the system's memory.
- There is no 1 MB limit in protected mode.
- Ability to multitask, meaning having the operating system manage the execution of multiple programs simultaneously.
- Support for virtual memory, which allows the system to use the hard disk to emulate additional system memory when needed.
- Faster (32-bit) access to memory and faster 32-bit drivers to do I/O transfers
- Each program that is running has its own assigned memory locations, which are protected from conflict with other programs.
- If a program tries to use a memory address that it isn't allowed to, a "protection fault" is generated.
- All of the major operating systems today use protected mode, including Windows 3.x, Window 9x, Windows NT, OS/2 and Linux.
- All processors from the 286 on can use protected mode.

**c) Name the different types of key-switches in keyboard. Explain the principle of working of opto-electronic switch.**
***(Types - 2 marks, Working - 4 marks, diagram - 2 marks)***

**Ans:**

**Keyboard Switches**

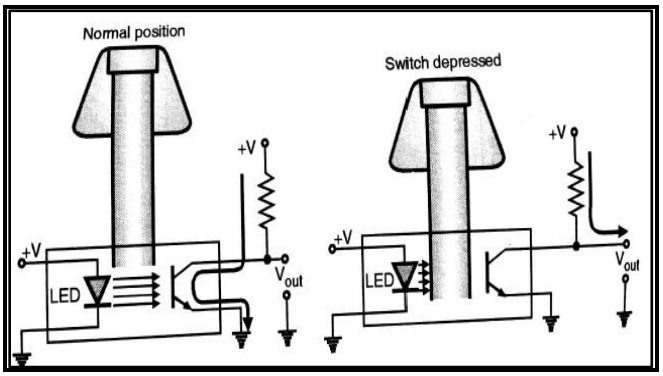
1. **Capacitive switch**
2. **Opto –electronic switch**
3. **Membrane switch**
4. **Mechanical switch**
5. **Rubber Dome switch**

**Opto-electronic switch:-**

In opto-electronic switch LED and Photo transistors are used.

LED generates light when proper electric power is applied and opposite to LED phototransistor is used. Phototransistor allows the current as long as light is applied to it. If light falling to phototransistor is removed, then current does not flow through it.

When the key is not pressed, light falls onto phototransistor, current flow through the phototransistor and produces very low voltage at the output **V**out.
When key is depressed light emitted from LED is blocked, which stops the current flow through phototransistor and a different value is produced at the output **V**out.




**6. Attempt any TWO of the following : 16**

**a) With suitable block diagram, describe construction of CDROM drive and explain the recording mechanism.**
***(Diagram - 2 marks; Description - 4 marks; recording mechanism - 2 marks)***

**Ans:**

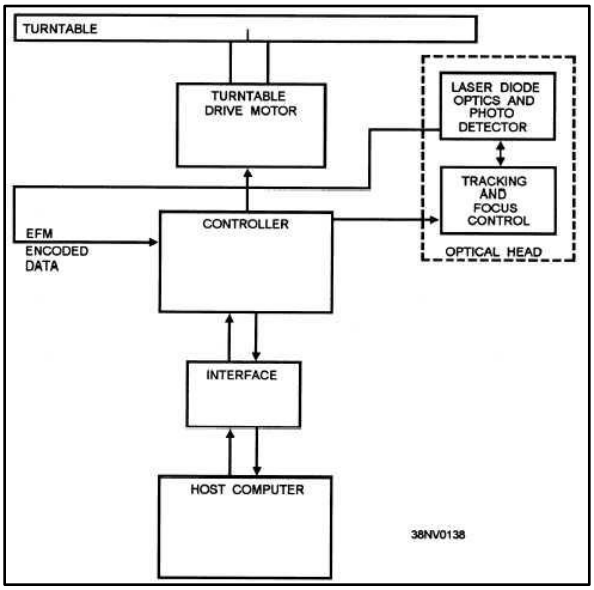
**CDROM DRIVE**
Compact Disc Read only Memory
Use to read CDROM, Connected to computer via IDE(ATA),SCSI,USB interface
**The basic components of the CD-ROM drive are the following:**

1. Optical head
2. Turntable
3. Computer interface section
4. Microprocessor based control system

The optical head contains the circuitry to read the data from the disc. This unit usually consists of four main subassemblies;

(1) The laser, used to generate a light beam;
(2) A lens system, to focus the laser beam on the disc and to direct the reflected light to the photo detector;

(3) A series of servomotors that controls the position of the laser and lenses to ensure proper racking and focus; and
(4) A photo detector that evaluates the reflected light and converts the light to electrical impulses.

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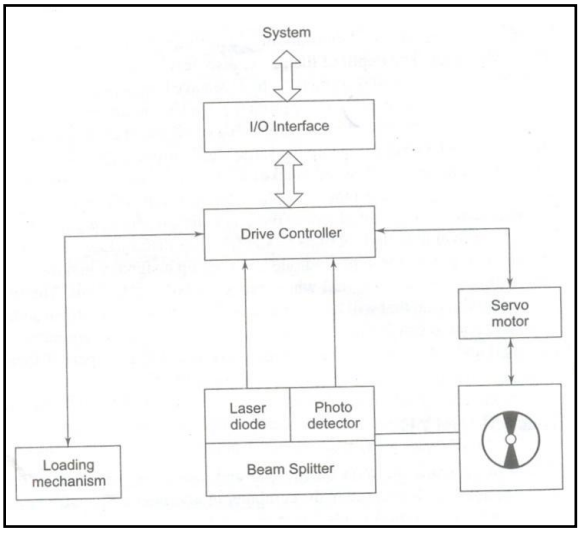


**TURNTABLE** The turntable rotates the disc and is driven by a servomotor. Since the data is written in a continuous spiral, the speed of the turntable must be adjustable so that the information passes over the optical head at a constant speed. The audio CD requires a speed of 1.3meters per second. This speed was adapted for use in computer applications, but proved to be extremely slow when compared to the processing and data transfer speeds of modem computers. The 2 X CD-ROM drives doubled the speed the data track passed over the optical head. The 4X, 6X, and 8X CD-ROM drives spin the disc even faster. The speed multiplication factor is based on the original speed of 1.3 meters per second.

**INTERFACE SECTION** The interface section provides for the transfer of data between the computer and the CD-ROM drive. Many CD-ROM drives are manufactured with the small computer systems interface (SCSI), although some proprietary interface units are available.

**CD CONTROLLER**

The CD controller processes the signals received from the optical head, attempts to correct any errors in the data, and controls the speed of the turntable. The information from the photodiodes that is received by the controller is still encoded in eight-to-fourteen modulation (EFM) data. The decoding of EFM data is done by the microprocessor. The code addresses a ROM that contains the proper byte for the encoded data. The output of the ROM is stored in a RAM where it is checked for errors.

Recording Mechanism:-

- The CD recording drive has a laser unit, which heats the organic layer which makes the hole (called as ‘pit’)
- Information recorded on CD using a series of pits . These pits are also called as bumps. The unmarked areas between pits are called lands.
- Lands are flat surface; the information is stored permanently as pits and land on the CD.
- Light reflected from pit to land or land to pit transition the intensity of reflected light changes.(logic 1) No change in intensity of light from pit of land is logic 0.
- EMF ( Eight to Fourteen modulation ) is an encoding technique used by CD.
- Data is broken into 8 bit blocks and each block is translated into 14 bit codeword using predefine lookup table.
- The 14 bit codeword chosen so that binary ones are always separated by minimum 2 and maximum 10 binary zeros.

**b) Give the eight specifications of blue-ray disk with typical value.**
***(Any eight; Each Specification -1 mark)***

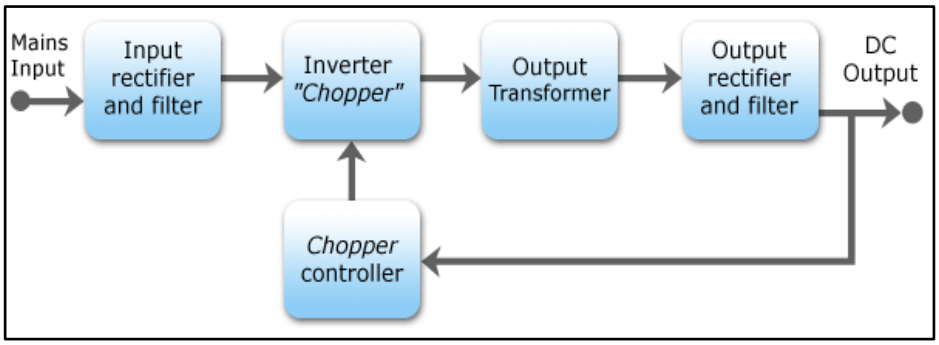
**Ans:**

| | |
|---|---|
| Capacity (Single Layer) | 23.3GB/25GB/27GB |
| Capacity (Dual Layer) | 46.6GB/50Gb/54Gb |
| Laser wavelength | 405nm (blue-violet) |
| Lens Numerical Aperture | 0.85 |
| Cartridge dimensions | Approx 129X131X7mm |
| Disc Diameter | 120mm |
| Disc Thickness | 1.2mm |
| Optical Protection Layer | 0.1mm |
| Tracking Pitch | 0.32μm |
| Shortest Pit Length | 0.160/0.149/0.138μm |
| Recording Density | 16.8/18.0/19.5 Gb/Sq. In |
| Data transfer rate | 36Mbps |
| Recording Format | Phase Change Recording |
| Tracking Format | Groove Recording |
| Video Format | MPEG2 |

**c) With suitable block diagram describe the working of SMPS.**
***(Diagram - 3 marks, explanation - 5 marks)***

**Ans:**

**Block Diagram of SMPS**

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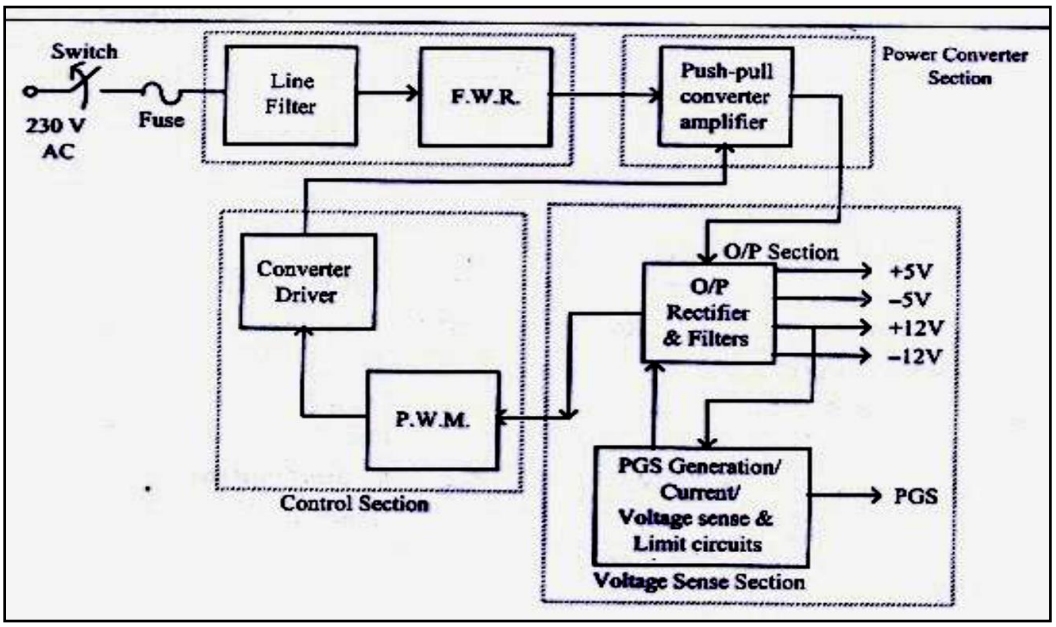

**Working of SMPS:-**

**Input rectifier stage**

If the SMPS has an AC input, then the first stage is to convert the input to DC. This is called *rectification*.

The function of the rectifier is to convert AC voltage into DC voltage. Here rectifier produces an regulated DC voltage which is then sent to a filter capacitor.

AC line voltage is first cleaned by removing Electromagnetic Interferences that may be introduced by external noise, EMI filter remove noise - AC input

Bridge rectifier and pi filter convert AC to DC and remove ripples, Unregulated DC fed as input to switching regulator;

**Inverter "Chopper" Stage (PWM)**

The series of square wave pulses produced by switching regulator (Chopper) are isolated, Chopper controller control ON and OFF time (width of square wave pulses). Inverter converts DC to AC which is then fed to transformer.

**Output transformer**

It is used to isolate output from input signal. This converts the voltage up or down to required output level.

**Output rectifier and filter**

AC output from transformer is rectified and the filter smoothens this output. Thus a pure DC voltage is obtained.

**Chopper controller**

This is used to maintain desired voltage level. The actual value is compared with reference voltage. If there is a difference found, the amplifier gives signal to (chopper controller) PWM controller. PWM controllers then adjust the ON period of switch so as to maintain the desired output voltage.